ABSTRACT OF THE DISCLOSURE

An integrated includes a test pattern generation unit, which divides a test pattern into scanning test patterns; scan chains, which shift in the scanning test patterns, output them to a logic circuit at the same time, input the test results from the logic circuit, and shift out them; and a test result compression unit, which is connected to the output stages of the scan chains, compresses the test results into the same number of compressed test result signatures as the test results, and outputs them to the scan chains in a first order that allows one-to-one mapping.